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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,666	12/31/2003	Hidcharu Koike	12057-US-PA	1665
31561	7590	09/09/2004	EXAMINER	
JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE 7 FLOOR-1, NO. 100 ROOSEVELT ROAD, SECTION 2 TAIPEI, 100 TAIWAN			WILLIAMS, HOWARD L	
			ART UNIT	PAPER NUMBER
			2819	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/707,666

Applicant(s)

KOIKE, HIDCHARU

Examiner

Howard L. Williams

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10-15 is/are allowed.
- 6) ☒ Claim(s) 1-9 is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|--|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date ____ | 6) <input type="checkbox"/> Other: ____ |

Claims 7 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In these claims the recitation of "the first subtractor" lacks antecedent. Alternatively, the claim nomenclature recites "second subtractor" before the appearance of a first subtractor, which is an inappropriate use of ordinal numbering. Changing the dependency of claims 7 and 8 would correct the situation.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-6 are rejected under 35 U.S.C. 103(a) as unpatentable over Deffendall et al. (US 4,337,456) in view of Eng, Jr. et al. (US 5,321,403).

The claim structure used is a bit unusual from common U.S. practice, typically the function of the elements is recited adjacent the respective elements. The claim as presented provides a rather choppy reading.

Deffendall et al. discloses a multi-channel dual slope ADC with digital offset correction. The input circuit with switches to supply the various input voltages or reference voltages is shown in dashed box 10 of figure 1. The integrator is illustrated as elements 32 and 34 in figure 1 and the comparator is of course element 44 also in figure 1. The offset cancellation logic, hysteresis logic, control logic, and data counter are embodied in microprocessor (CPU 54; fig. 1). The offset value is determined in the first cycle (t_2 and t_0 ; fig. 2) and stored in memory (col. 6, lines 25-27). The subtraction of the offset can be effectively accomplished by setting the counter to a value corresponding to $-t_0/k$ at the start

of a measurement cycle (col 6 line 63-col. 7 line 5). The recited hysteresis logic is only given the function of determining the output value in these claims and the microprocessor of Deffendall et al. clearly does that. Regarding claim 5, Deffendall et al. does not specify that the comparator has hysteresis. Eng Jr. et al. teaches using a comparator with a slight hysteresis (col. 4, lines 20-30) to improve to avoid comparator oscillation for small inputs and thus shallow ramps. It would have been obvious from the teaching of Eng, Jr. et al. to use a comparator with slight hysteresis in Deffendall et al. to avoid comparator oscillation and indecision as taught by Eng, Jr.


Claims 10-15 allowed.

Claims 7-9 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gray (US 5,262,780) teaches an integration based ADC which occasionally determines the amplifier offset and digitally stores the measured offset for compensation of routine conversions.

Any inquiry concerning this communication should be directed to Howard L. Williams at telephone number 571-272-1815.

9/2/04


Howard L. Williams
Primary Examiner
Art Unit 2819